



ALTERNATIVE TO PTO/SB/08A/B (09/06)

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	10/713,729
				Filing Date	November 13, 2003
				First Named Inventor	Bruce W. MCGAUGHY
				Art Unit	2128
Examiner Name	D. Silver				
Sheet	1	of	1	Attorney Docket Number	188122001700

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/D.S./	1.	US-2003/0237067-A1	12-25-2003	Mielke et al.	
	2.	US-2004/0078767-A1	04-22-2004	Burks et al.	
	3.	US-4,942,536-A	07-17-1990	Watanabe et al.	
	4.	US-5,910,898-A	06-08-1999	Johannsen	
	5.	US-6,026,226-A	02-15-2000	Heile et al.	
	6.	US-6,035,107-A	03-07-2000	Kuehlmann et al.	
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	11.	US-6,449,761-B1	09-10-2002	Greidinger et al.	
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	13.	US-6,807,520-B1	10-19-2004	Zhou et al.	
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Examiner Initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)					

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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	15.	Chakrabarti, D.R. et al. (November 23-24, 1995). "An Improved Hierarchical Test Generation Technique for Combinational Circuits with Repetitive Sub-circuits," <i>Proceedings of the Fourth Asian Test Symposium 1995</i> , 1:237-243.	
	16.	Jones et al. (February 1994). "A Cache-Based Method for Acceleration Switch-Level Simulation," <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> 13(2).	
	17.	Stanford.edu. "Radix 2 FFT Complexity is N Log N," <i>In Mathematics of the Discrete Fourier Transform (DFT) with Music and Audio Application</i> . Smith, III, J.O. (2003). W3K Publishing: Stanford, located at < http://cma.stanford.edu/~jos/mdft/Radix_2_FFT_Complexity.html >, 1 page.	
	18.	Wong, Y. (1985). "Hierarchical Circuit Verification," <i>IEEE 22nd Design Automation Conference</i> .	

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Examiner Signature	/David Silver/ (02/01/2008)	Date Considered	
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